**Assignment 1; Week 1**

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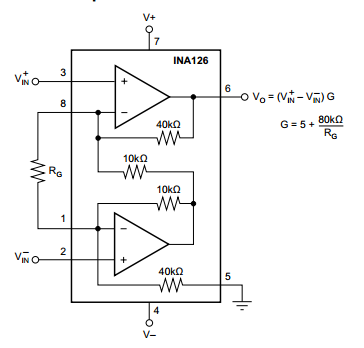
**\*RD-1: For a real design problem, consider an available industry IA. Referring to the circuit topology shown in the INA126 datasheet, analyze the circuit to verify the manufacturer’s gain equation**

Figure 1 - IA126 Circuit for Problem RD-1

Where

V1

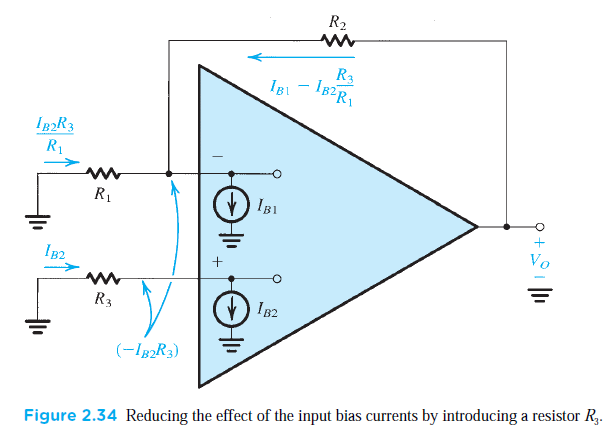
In this sense, the equation can be manipulated to show

In normal noninverting circuits, the equation is represented as where the “1” represents that the closed-loop gain of a non-inverting amplifier will always be greater but never less than 1. Respectively, the closed-loop gain of this circuit will never be less than 5.

As such, the 80kΩ value derives from the real resistors in the equation. The equation used to analyze this circuit can be shown and, in the end, should match the equation above.

**\*RD-2: For modern op amps with ib on the order of pA, do you think explicit ib compensation—e.g.,**

**R3 in Fig 2.34, is necessary? Why or why not?**



The resistor represented by R3 in Figure 2.34 is an example of an input bias resistor. This is such that the two input terminals of the op amp have input bias current travelling into them. While ideal op amp circuits assume that input resistance is infinite, a real op amp has a finite value. With this finite value, the bias current is one that adds noise and provides a difference to the DC output voltage.

(From a signal point of view, R3 has nearly no effect on the input or output gain of the circuit.)

The R3 resistor provided for the input bias current allows a reduction of the output dc voltage that occurred due to the current. Additionally, the input bias resistor on the noninverting terminal allows an evaluation of the effect of a finite offset current. In conclusion, while the resistor is not necessary, the resulting output voltage is typically a large value smaller than the value obtained without R3. As such, to minimize the effect of the input bias currents, a resistance equal to the dc resistance should be placed by the noninverting and inverting terminal.

**\*2.9 Inverting Amp, resistor tolerance**

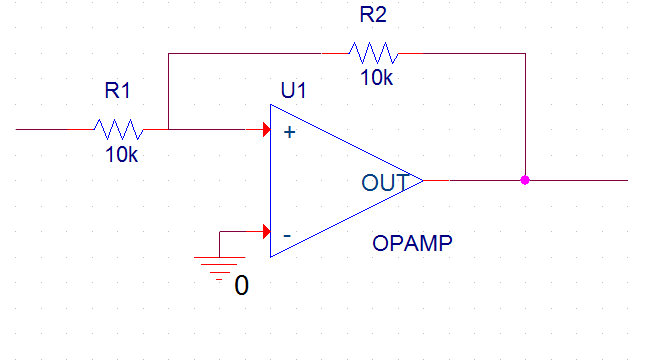
A particular inverting circuit uses an ideal op amp and two 10kΩ resistors. (a) What closed-loop gain would you expect? (b) If a dc voltage of +1.00 V is applied at the input, what output result? (c) If the 10-kΩ resistors are said to be “1% resistors,” having values somewhere in the range (1 ± 0.01) times the nominal value, what range of outputs would you expect to actually measure for an input of precisely 1.00 V?

Figure 2 – Op Amp circuit for Problem 2.9

As with inverting operational amplifier circuit shown in Figure 2, the gain is represented by the circuit below:

1. With the circuit and equation provided above, the expected gain of the circuit would be 1 V/V with the equation shown to be
2. If a dc voltage of +1.00 V is applied at the input of the circuit, the output of the circuit would be -**1V.**

Since Vi = 1V…

Where and *A = -1 V/V*

1. If the 10-kΩ resistors are said to be “1% resistors,” having values somewhere in the range (1 ± 0.01) times the nominal value, the range of the outputs would be **V.**

Work shown below.

Since Vi = 1V…

Plug in 1 ± 0.01 for R2 and R1 between the range for Vo

**\*D2.42 Diff Amp design**

In an instrumentation system, there is a need to take the difference between two signals, one of *v*1 = 2 sin(2π × 60*t*) + 0.01 sin(2π × 1000*t*) volts and another of *v*2 = 2 sin(2π × 60*t*) − 0.01 sin(2π × 1000*t*) volts. Draw a circuit that finds the required difference using two op amps and mainly 100-kΩ resistors. Since it is desirable to amplify the 1000-Hz component in the process, arrange to provide an overall gain of 100 as well. The op amps available are ideal except that their output voltage swing is limited to ±10 V.

This circuit requires a differential amplifier using two operational amplifiers. As such, the circuit for this problem should look like Figure 3 below.

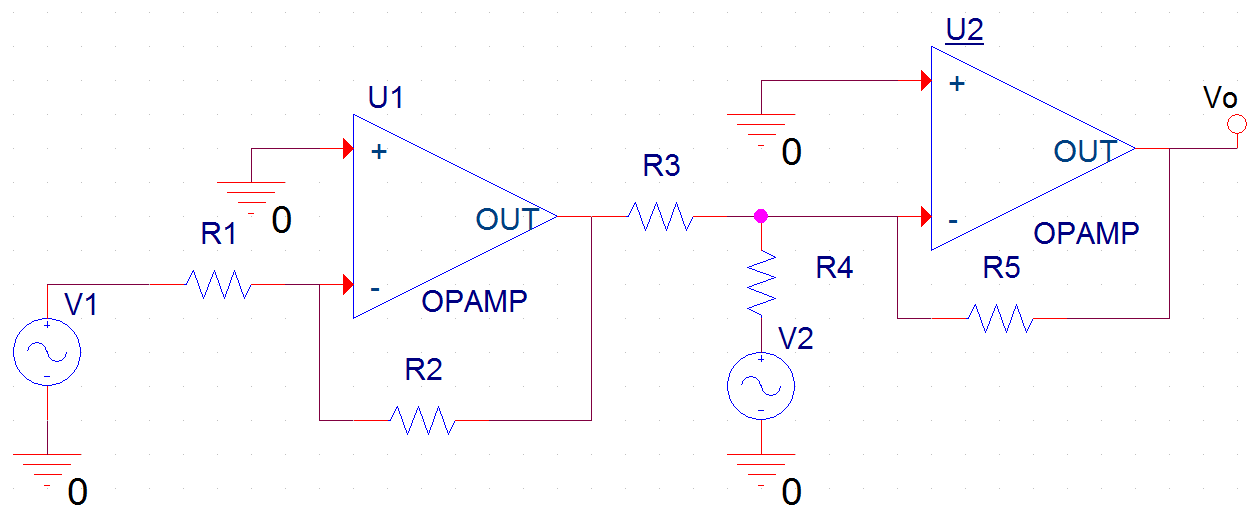


Figure 3 - Two-stage differential amplifier

After this circuit has been produced, the analysis of this circuit may begin. In the op amps of the circuit, each use the inverting terminal of the device. Respectively, the first output of the first op amp is

The second amplifier, U2, acts as an amplifier that takes the sum of the two voltages and the output of the inverting and noninverting terminals. The output of the summing amplifier is…

However, Vo1 simply equals Vo of the first amplifier. In this case, the following equation is used.

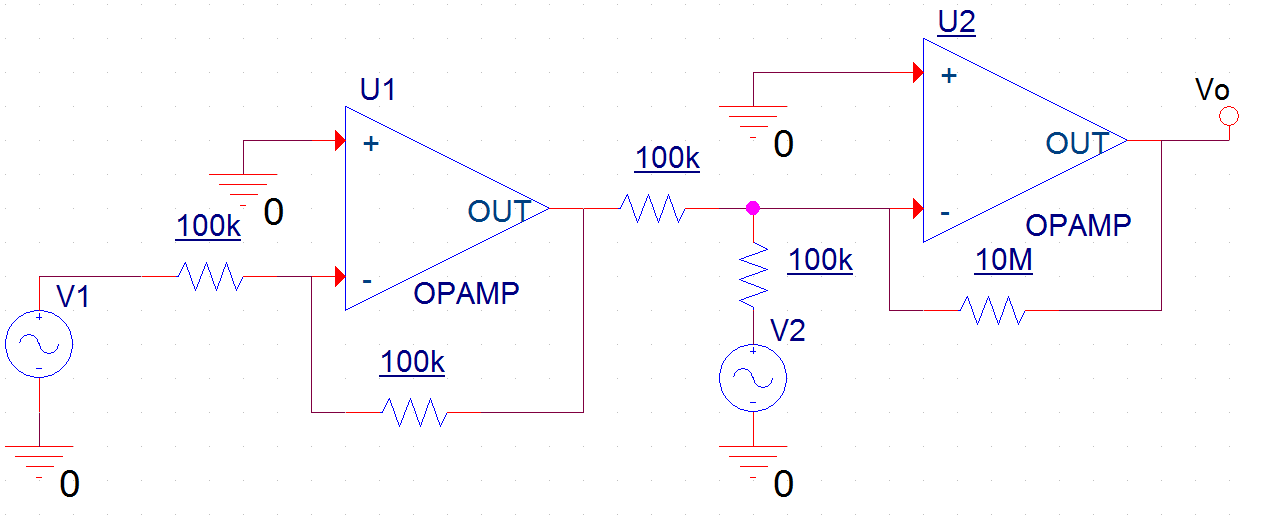
Where = 100 V/V as given

Because the resistance values call for mostly 100kΩ values, R1 – R4 should be 100kΩ. However, this does not produce a gain of 100. Assuming R4 is 100kΩ, R5 = MΩ

To check this, the difference between the two input voltages is,

With a gain of 100V, the output voltage is,

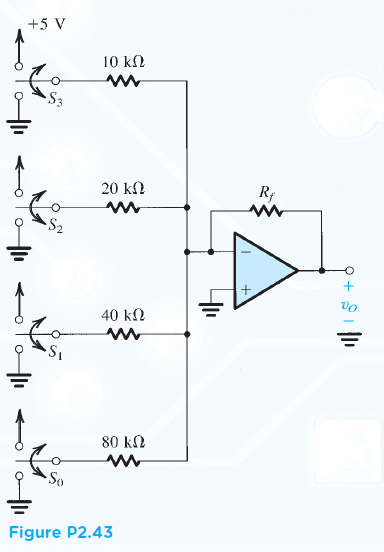
In turn, this voltage configuration aligns the output voltage to **±2** which is below the limit of 10.



**\*2.43 IDAC; change to achieve 0** ≤**Vo** ≤**-3.3V**

Figure P2.43 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary

word *a*3*a*2*a*1*a*0, where *a*0, *a*1, *a*2, and *a*3 take the values of 0 or 1, and it provides an analog output voltage *vo* proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if *a*2 is 0 then switch *S*2 connects the 20-kΩ resistor to ground, while if *a*2 is 1 then *S*2 connects the 20-kΩ resistor to the +5-V power supply. Show that *vo* is given by

 where *Rf* is in kilohms. Find the value of *Rf* so that *vo* ranges from 0 to −3.3 volts.

According to the DAC of the circuit in 2.43, the output voltage for the summing amp is

Here the power supply voltage is multiplied by each input binary word. As such, vn is replaced by 5an and Rn is replaced by its respective resistor.

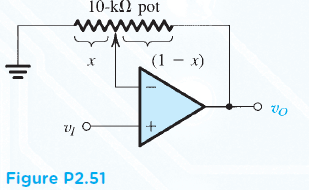
Substitution results in…

Assuming Rf is a kiloohm measurement…

To calculate Rf from 0 to -12V, the assumption that a3a2a1a0 = 1001 must be made at -3.3V. As this occurs, the equations follow this form.

**\*D2.51 Var gain using pot**

The circuit shown in Fig. P2.51 utilizes a 10-kΩ potentiometer to realize an adjustable-gain amplifier. Derive an expression for the gain as a function of the potentiometer setting *x*. Assume the op amp to be ideal. What is the range of gains obtained? Show how to add a fixed resistor so that the gain range can be 1 to 11 V/V. What should the resistor value be?

The expression of this circuit shown in Figure 2.51 represents two resistors split between the 10-kΩ potentiometer where R1 is x and R2 is (1-x).

Due to the potentiometer being on a noninverting op amp input, the equation is as follows.

Therefore if , x =1 and the range of the op amp is and

or

At the maximum and minimum of 1 and 11, the Resistors can be found as shown below. Adding a fixed resistor of 5k produced a value of for R1

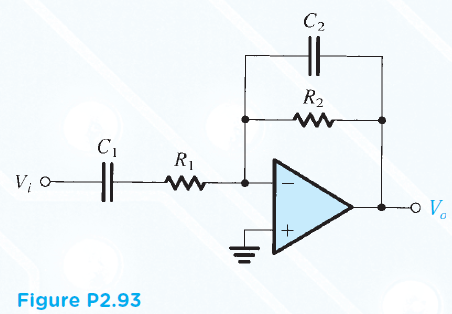
**\*D2.93 H(s) for op amp, Bode plot**

Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be

written in the form

where ω1 = 1/C1 R1 and ω2 = 1/C2 R2. Assuming that the circuit is designed such that ω2 >> ω1. find approximate expressions for the transfer function in the following frequency regions:

1. ω << ω1
2. ω1 << ω << ω2
3. ω >> ω2



Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high frequency end in the manner of a low-pass STC network.

Design the circuit to provide a gain of 40 dB in the “middle frequency range,” a low-frequency 3-dB point at 100 Hz, a high-frequency 3-dB point at 100 kHz, and an input resistance (at ω >> ω1) of 1 kΩ.

With two pairs of impedances in series and parallel respectively, the equation follows.

Removing the j and simplifying the equation after dividing produces a transfer function matching the expected result.

1. ω << ω1

When ω << ω1, and ω1 << ω2, produces a value close to 0. As such, the equation is simplified.

For ω << ω1

1. ω1 << ω << ω2

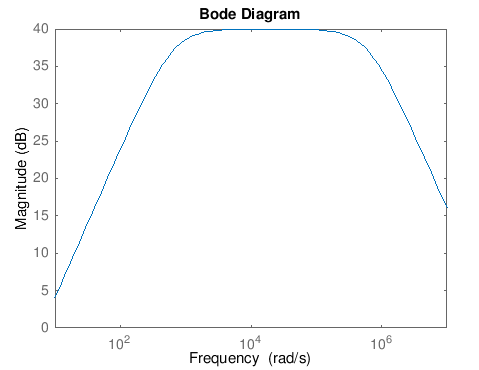
When ω1 << ω << ω2, and produces a value close to 0. As such, the equation is simplified.

For ω1 << ω << ω2,

1. ω >> ω2

When ω >> ω2, and produces a value close to 0. As such, the equation is simplified.

For ω >> ω2,

Given a gain (A) in decibels is 40 dB, the voltage gain follows

Therefore, when ω1 << ω << ω2, and R1 = 1kΩ, (input resistance)

Calculate angular frequency

Calculate capacitance

Plugging into yields the Bode plot shown to the right

**\*2.95 Eos + signal**

A noninverting amplifier with a gain of 200 uses an op amp having an input offset voltage of 2 mV. Find the

output when the input is 0.01 sin ω*t*, volts.

**\*D2.117 Cascading amps**

This problem illustrates the use of cascaded

closed-loop amplifiers to obtain an overall bandwidth

greater than can be achieved using a single-stage amplifier

with the same overall gain.

1. Show that cascading two identical amplifier stages, each having a low-pass STC frequency response with a 3-dB frequency *f*1, results in an overall amplifier with a 3-dB frequency given by
2. It is required to design a noninverting amplifier with a dc gain of 40 dB utilizing a single internally compensated op amp with *ft* = 1 MHz. What is the 3-dB frequency obtained?
3. Redesign the amplifier of (b) by cascading two identical noninverting amplifiers each with a dc gain of 20 dB. What is the 3-dB frequency of the overall amplifier? Compare this to the value obtained in (b) above.

**\*D2.127 The compleat op amp designer**

In designing with op amps one has to check the

limitations on the voltage and frequency ranges of operation

of the closed-loop amplifier, imposed by the op-amp finite

bandwidth ( *ft*), slew rate (SR), and output saturation (*Vo*max).

This problem illustrates the point by considering the use of

an op amp with *ft* = 2 MHz, SR = 1 V/μs, and *Vo*max = 10 V in

the design of a noninverting amplifier with a nominal gain

of 10. Assume a sine-wave input with peak amplitude *Vi*.

1. If *Vi* = 0.5 V, what is the maximum frequency before the output distorts?
2. If *f* = 20 kHz, what is the maximum value of *Vi* before the output distorts?
3. If *Vi* = 50 mV, what is the useful frequency range of operation?
4. If *f* = 5 kHz, what is the useful input voltage range?